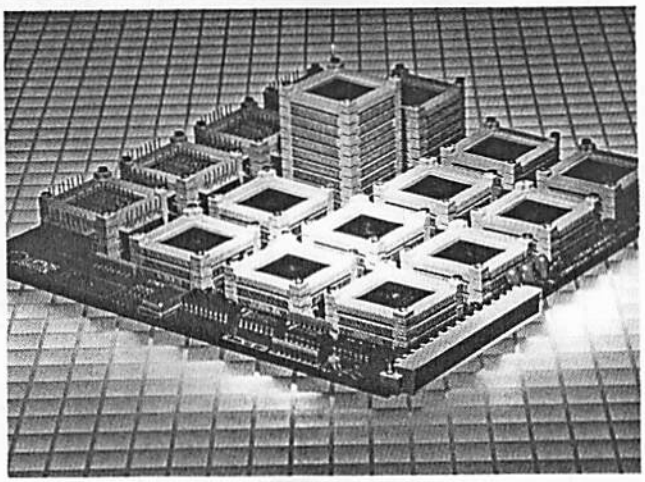

Partitioning–The Chiprack Solution

A method of partitioning large electronic assemblies by using interconnected stacks has been developed by Dowty Interconnect. A system employing the technology, known as the Chiprack system, is described by *Mike Anstey*.

The very high densities of circuitry made possible with surface mount devices, often present assembly, test and repair problems on boards, even as small as a Eurocard. Partitioning of the circuitry into smaller and more easily manageable sub-assemblies has been identified as a possible solution and a number of approaches to partitioning have been proposed.

The DTI funded HIT (Hierarchical Interconnection Technology) Project (*EP, Nov/Dec, 1987*) proposes the partitioning of a circuit onto a number of smaller 'Child' boards which are then mounted flat onto the surface of a larger interconnecting 'Motherboard'. These smaller boards are of manageable size for automated handling in production and for accessing during test procedures. They may also be replaced in modular fashion when a failure occurs rather than the entire board assembly.

Another approach has been adopted by Dowty Interconnect in their 'Chiprack' system launched at the start of this year. This system also partitions a circuit into smaller circuit assemblies. These sub-assemblies may be as small as a single Very Large Scale Integrated (VLSI) circuit or as large as one of the HIT 'Child' sub-assemblies. The main difference with the subsequent assembly process is that the 'Chiprack' sub-assemblies are then stacked and interconnected by means of the Chiprack connectors.

Carriers and Connectors

Chiprack carriers are of two types. In many Chiprack systems the carriers are leadless chip carrier integrated circuit packages and hold a single VLSI circuit (Fig 1a). Alternatively, however, small PCB or other boards may hold a number of surface mount or COB (Chip on Board) components and in this case they resemble hybrids or the small surface mount assemblies employed by HIT (Fig 1b). (All Chiprack carriers and boards have contacts on both upper and lower surfaces and may be fabricated in encapsulating plastics and resins, FR4 materials and ceramics.)

The Chiprack connectors have been designed to both stack and interconnect the carriers (Fig 2). The upper surface of one carrier is directly connected to the lower surface of an adjacent carrier by means of the connectors. The connector contacts present all signals passing between carriers to the outside of the stack and provide a heat path from inside to outside. The exterior of an interconnected stack looks and behaves as a convoluted heat sink.

Construction of an electronic product is simply a matter of arranging the carriers and connectors into a stack and clamping or fixing the resulting assembly. Prototyping connectors are clamped together by means of torque bars whereas production connectors will snap together permitting high mechanised assembly rates (typically only a few seconds to assemble a completed product).

Signal Tracks

Clearly signals and power may be bussed through a stacked assembly. However what is often overlooked is that the intersection of each carrier in the assembly permits signals to be re-routed at that intersection. This permits complex signal tracking in a single stacked assembly.

Application Specific Circuits (ASICs) may be used to implement any SSI or MSI logic in a system and to implement signal routing. It therefore becomes possible to route all the signals in a system on the silicon structures within the system.

The availability of all signals on the outside of stacks presents a range of three dimensional interconnection possibilities between stacks. Signal routing possibilities are given in Figure 3.

System Installation

The 68070 computer system, recently installed at CLCC Electronics, consists of a number of component carriers and connectors which, when stacked together, form a very compact microprocessor system (Fig 4). The carriers, in order of arrangement in the stack, are:

1. RS232 Interface.
2. 68070 Central Processing Unit (CPU).
3. Application Specific Integrated Circuit (ASIC).
4. Read Only Memory (ROM).
5. Random Access Memory (RAM).

System design started with the drafting of a hardware and software specification for a 68000 series system. Then, in a departure from normal practice, a search was conducted to identify monolithic silicon 'building blocks' to meet the project requirements. The Chiprack system is best employed to interconnect few VLSI circuits with any small and medium

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scale logic 'mopped up' into a single ASIC.

The Philips 68070 processor was an ideal starting point in that it not only comprises a 68000 series processor, with well established software support, but in addition many of the peripheral functions, normally provided by separate chips, have been integrated onto the same die.

The project requirements specified the possibility of battery support and therefore static memory was chosen and the largest readily available memories were identified as 32K×8. It was decided that the initial design should use 2×32K×8, configured as 32K×16, for each of the memory carriers, but that future expansion should be provided by permitting up to four 128K×8 per carrier, configured as 256K×16.

The memory interface could have been implemented on a single carrier using a hybrid solution but it was decided that an ASIC would be a superior solution, and even in small

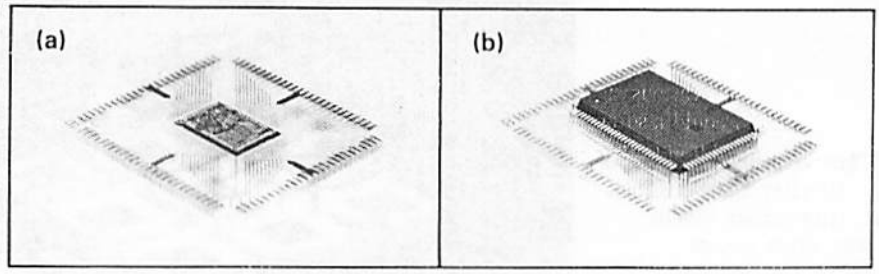

Fig. 1. (a) Chiprack leadless chip carrier, (b) Chiprack 'hybrid' carrier.

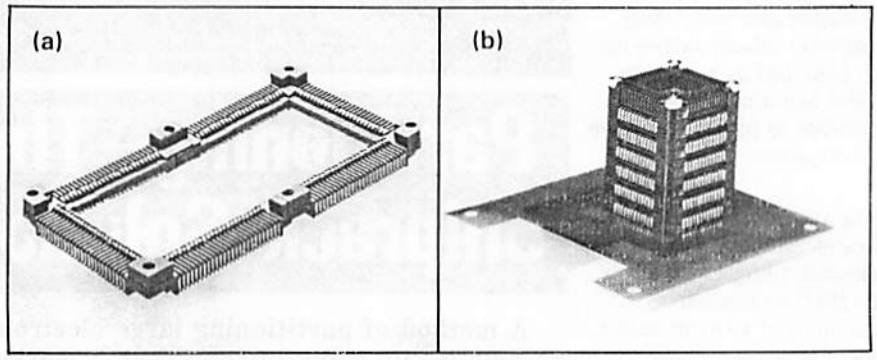

Fig. 2. (a) Chiprack connector, (b) Chiprack assembly.

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volumes, could also be cost effective. In addition to the memory interface, the ASIC would provide various signals to the processor and could also be used for routing signals to appropriate positions in the stack, if required.

An RS232 interface to the system was required and in order to simplify power supply requirements, a charge pump device (MAX232) was chosen to generate RS232 levels from the 5V supply.

The next step in the project was to produce circuit diagrams and then to construct a wirewrap prototype in traditional PCB board technology, a step which proved in the end to be unnecessary.

The circuit was then partitioned into major functional areas and the contents and ordering of the carriers decided on the basis of convenience of construction. It had, for example, been decided that memory should be expandable by the addition of additional carriers and therefore memory was postitioned at one end of the stack.

The planning of signal paths through the Chiprack structure could, ideally, be optimised by use of CAD. With small modification, some of the multilayer PCB design packages could have been employed. The regularity of signal patterning out of the 68070, however, indicated that the task could be carried out by hand. A special design sheet was produced and the signal tracking mapped directly onto the sheet using a simple coding scheme.

The netlist of connections generated by the production of the signal tracking sheet then permitted the CAD design of each of the carriers in the system using a standard PCB design software package. The remainder of the project followed normal procedures of manufacture, assembly and test.

System Features

•Working systems are easily and rapidly assembled and hand assembly rates of 2–3 systems a minute, using minimal aids and jigs, are possible. Mechanised assembly involves two operations, the simultaneous placement of the carriers and connectors into a former, and then the compression of the sub-assemblies into a functional electronic unit. Very high assembly rates are expected.

•The highly modular nature of the system facilitates alteration or enhancement. For example, the processor and ASIC carriers could be replaced with a different, or an upgraded processor and interface. Additional memory carriers may be added or existing carriers replaced with larger capacity carriers.

•Test and repair of systems is simplified. All the carriers have a constant 'footprint', in common with the assembled system, for ease of attachment to test instruments. Malfunctioning systems are easily taken apart for replacement of faulty carriers.

•The system is both compact and robust. The 512K byte 68070 microcomputer system complete with I/O facilities is approximately 112 cc (7×4×4 cm). The 2M byte system is expected to be the same size.

•Signals are available at ends and sides of the assembly, presenting unusual opportunities to similar assemblies or peripheral devices (e.g. a liquid crystal display could be driven from a link to the side connections on the assembly). The construction of three dimensional arrays of assemblies is facilitated by the incorporation of electronic or optical communications links.

Current applications may be categorised into single stack applications and multi-stack/array applications.

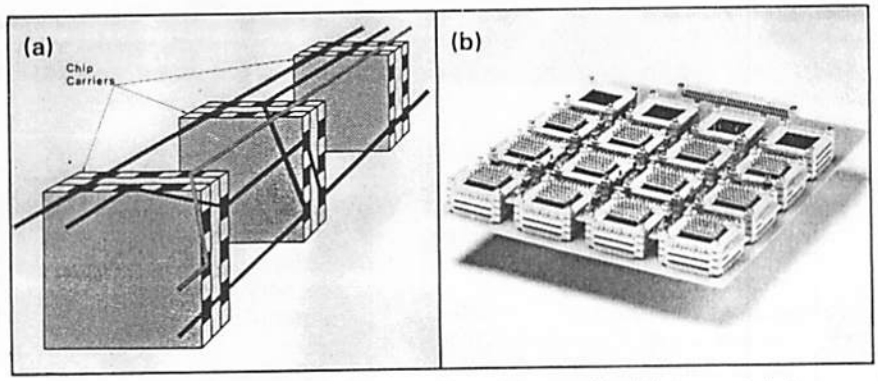

Fig. 3. Signal routing possibilities (a) in a single stacked assembly, (b) between stacked assemblies.

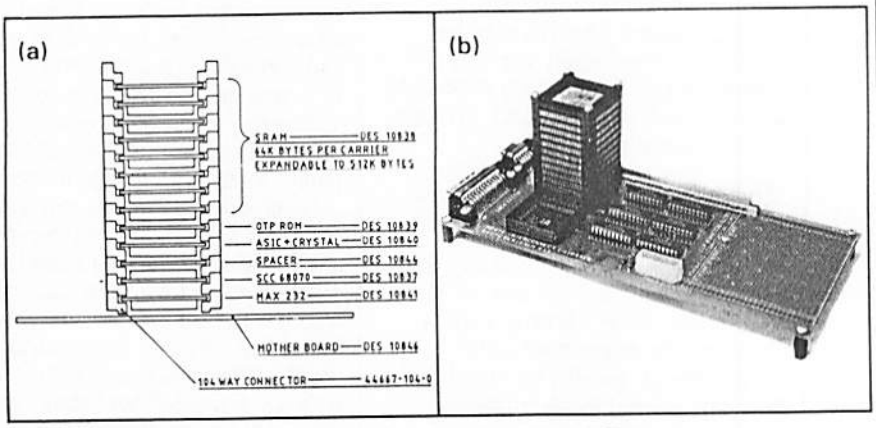

Fig. 4. (a) 68070 System diagram, (b) perspective view of 68070 System.

Single Stack

Form factor. The shape of Chiprack suits certain applications (e.g. hand held data loggers/test instruments) and the shape coupled with minimal volume enables considerable processing power to be placed in 'difficult' locations e.g. down boreholes. These are often also situations where high bandwidth input signals need to be processed close to the sensor and low bandwidth data extracted for manageable onward transmission.

Modular Expansion. Chiprack systems can be used in conjunction with board technology to create modular expansion capabilities. Boards designed to fit established bus systems may be designed to hold, for example, Chiprack memory carriers. Expansion of the memory now becomes possible by stacking on further

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Chiprack carriers. Thus, not only is the complete board real estate fully populated but further expansion becomes possible by upward stacking rather than by a board redesign.

Modular Replacement. Products designed around Chiprack assemblies may exploit the highly modular design by offering modular replacement of one or more of sections of the Chiprack assembly. Established hardware (e.g. casings, displays, keypads) may be retained whereas rapidly evolving silicon technology may be upgraded in modular fashion as and when required, giving a much extended product life.

Multiple Stack/Array

A single stack Chiprack assembly consisting of a processor, memory and communications facilities may be termed a processing 'node'. Arrays of these nodes may be constructed and communication enabled by use of the three dimensional freedom offered. Electronic or optical communication links may be employed at either end, or at any level in a node, to link the node to adjacent nodes. The ability to be able to add processing power incrementally, by the addition of nodes, or to be able to expand existing nodes by the addition of memory, are seen as attractive features of systems constructed in this manner.

Neighbour to nearest neighbour communications imposes limitations in large arrays of nodes because any communication has to be passed through all intermediate nodes between source and destination. It is however possible to incorporate electronic or optical 'highways' which could establish point to point links between geographically remote nodes within large arrays.

Single stack assemblies may also be composed or a number of separate processors and associated memories. A double extended eurocard size board arranged to take a 4×4×4 array of transputers has been constructed. The board has expansion possibilities of between 1 and 64 transputers, with or without 0.5 to 32 Megabytes of memory. It would, of course, be possible to construct much larger arrays.

The Chiprack system offers the potential to reduce designs to few, large silicon 'building blocks' which may then be interconnected using simple, regular interconnecting structures. Initial design requires greater design effort and computer input but assembly times for the resulting systems are greatly decreased.

Editorial Notes

1. The Philips 68070 processor system which includes a set of Chiprack carriers is available in the form of a designer kit from Dowty Interconnect. Dowty is based in High Wycombe, Buckinghamshire. Tel. 0628 810810.

2. A range of products manufactured by Dowty will be on show at this years Internepcon Exhibition, Stand 5748.