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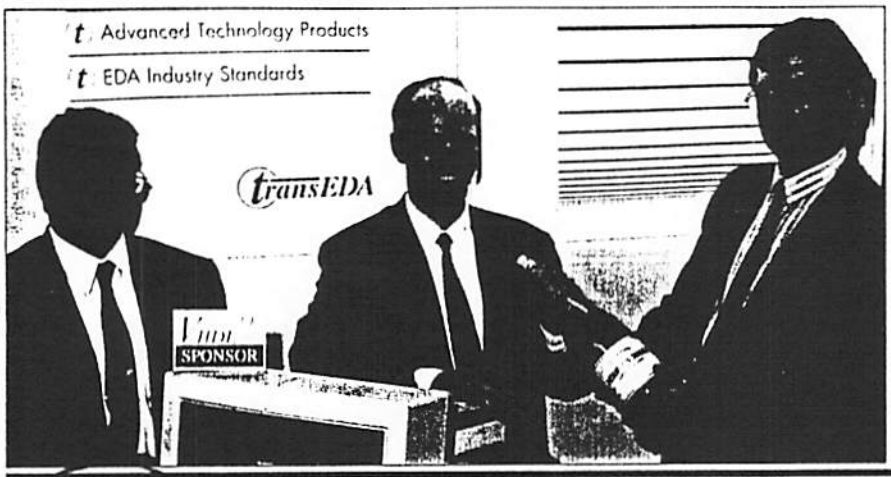

Champagne and chips...Paul Cornfield (centre), a systems engineer at British Aerospace Space Systems, has good reason to smile. As the winner of the design competition sponsored by TransEDA, Texas Instruments and *Electronics Weekly* at last week's Silicon Design Show, Cornfield walked off with two magnums of champagne and more than £30,000 worth of synthesis and FPGA design software. The competition asked entrants to submuit a behavioural-level design written in the VHDL language. Cornfield's winning entry, a digital filter, used advanced features of VHDL, including VHDL generics. At the show the design was synthesised to gate level using TransEDA's TransGATE software and then implemented in a TI TPC12 FPGA. Pictured with Cornfield are Mohan Maheswaran (left) TI's European FPGA technical marketing manager, and James Douglas, managing director of TransEDA.

UK first for PC in a cube

Engineers at Cambridge University have built a PC using a revolutionary PCB interconnection system.

The engineers, from Chiprack Electronics, built the 486 PC based on the Chips and Technologies chip set which was mounted on five multilayer PCBs. The PCBs were stacked one above the other using a patented connector system which was made under licence by Harwin.

The complete PC, including RAM and ROM, occupied a 50mm cube. Heating was not a problem, because the multilayer PCBs and the edge connectors acted as a heat sink. Chiprack expects to launch it first PC product next Spring and Harwin, which is in production with the connector, expects to sell it into a number of embedded applications.

Transputer hit by German pull out

German parallel supercomputer maker Parsytec is axing Inmos' T9000 transputer from its future machines because of continued delays in bringing out devices that perform to promised specifications.

The news, from one of Inmos' biggest customers, is a major blow to the SGS-Thomson subsidiary.

Sources close to Parsytec say that it has informed customers that forthcoming machines will use the 601 PowerPC chips from Motorola and IBM as processing elements. The sources suggest that older T800 transputers will still be used to handle communications between the processors.

Motorola has confirmed that Parsytec's Parix operating system is being ported to the PowerPC and that it will be used in a parallel processing machine built by Motorola's own computer group.

Parsytec refused to comment on specific product plans but a company spokesman confirmed that private discussions with major customers are taking place.

Parsytec has been one of the transputer's leading supporters. It announced T9000-based systems more than two years ago but was unable to build them because silicon did not appear until this year.

Even now, according to sources at several transputer customers, the T9000 can operate at only 10MHz, instead of the 50MHz originally intended, and half as fast as the 20MHz that Inmos promised this year.

Some sources add that not all of the instructions in the T9000's set are working properly yet, and that "supplies have dried up" because of the switching of manufacture from Wales to SGS-Thomson's new plant in Crolles, France.

Several transputer users have already turned to alternative processors. Parallel processing specialist Transtech is using Intel's i860 while it waits for T9000's. Meiko, a Bristol-based supercomputer maker, has started building machines with Sparc microprocessors.

Transtech insists that the T9000 is still part of its plans. "We would use the T9000 if we had any," said marketing manager Steve Hutton, "but it will be next year before we see any useful silicon." David Watson, managing director of Parsys, another parallel processing company, also confirmed his company's support for the T9000.

Inmos confirmed that current T9000 samples operate at 10MHz and are made at Newport. Samples from Crolles will become available in Q1 next year.

Microchip 'summit' plans half-micron CMOS ruling

A microchip 'summit union' between Europe's leading chip companies will produce a standard set of design rules and cell libraries for half-micron CMOS.

The companies involved are Philips, SGS-Thomson, Siemens, GEC-Plessey Semiconductors, Matra MHS, Mietec and European Silicon Structures (ES2).

The intention is to give potential customers the design rules for half-micron CMOS before the end of this year. Small quantity production of prototypes should be possible by April 1994 with full-scale production by April 1995.

Future intentions include developing and transfering a 0.35-micron process to all industrial partners in June 1995 so that they can deliver 0.35-micron Asics before the end of 1996.

The 'summit union' series of projects is being carried out under the Jessi project and the 1996 deadline coincides with the Jessi expiry date.

It is anticipated that the first companies to offer prototype half-micron Asics in 1994 will be Siemens, Philips, SGS-Thomson and Matra MHS and that GPS, Mietec and ES2 will follow a few months later.

Marconi runs GaAs low voltage process

GEC Marconi has run first wafers through its new low voltage gallium arsenide (GaAs) process which is intended to produce RF components for mobile telephones.

The first 3V devices will be ready for testing within a few weeks. They are expected to be power amplifiers and RF switches for the 1.8GHz frequency band used by the DCS1800 and DECT mobile telephone protocols.

A spokesman for GEC Marconi Materials Technology at Caswell said: "Hopefully we will have the low voltage process in place this time next year."

The 3V devices are the first results of a two year collaboration between GEC Marconi, BNR Europe and Bradford University.

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