Service Layer. The service layer generates essential clock wave forms required by the processor and elsewhere. This layer is implemented using a number of MSI devices and discrete components.

Processor layer. This layer contains only the F8680 device. Since the connector employed in this example provides 160 interconnections in the upward and in the downward direction, all processor signals can be made directly available to layers above or below the processor.

ROM and graphics RAM layer. This layer bears non-volatile memory which holds the low-level PC operating system (BIOS), and a static RAM device which serves as a graphics memory for the display controller available in the F8680.

Memory layer. This layer accommodates the main system RAM. Early trials made use of static RAM devices allowing 256 K Bytes per layer. A special design technique facilitated by the connector was used to allow a number of identical RAM layers to be stacked, allowing easy expansion of memory capacity.

I/O layer. This layer comprises a multi-function peripheral controller device intended for use in portable computer designs. It furnishes a parallel port, two serial ports, and support for diskette drives or hard disk.

For many embedded applications, an assembly consisting of the first four layers listed could fulfil the necessary functions. However, addition of the fifth layer provides significantly increased I/O capabilities, allowing the assembly to be substituted in place of a conventional desktop computer. A mother board provides a physical support for the five stacked layers, and is a convenient site on which to mount connectors to permit the experimental system to be used with standard peripheral devices. Further details of the design considerations and areas of application of the embedded PC described here are given in Holburn et al (2).

No fundamental changes in design procedure were occasioned by the use of the partitioning strategy described. In the first place the system was partitioned into major functional areas and the content and ordering of the carriers determined on the basis of convenience of construction. It had, for example, been decided that memory should be expandable by superposition of additional carriers, and therefore memory was positioned at one end of the stack.

Advantages

A number of important advantages arising from the use of this philosophy have been identified. These offer clear benefits for the designer, the manufacturer, the service engineer and the end-user. In addition, as a result of this approach to design, components and sub-

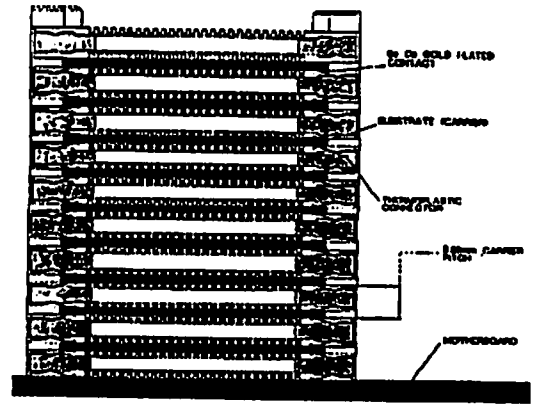

Figure 1: General arrangement

assemblies may readily be reused in alternative products.

Partitioning. The system is partitioned at a functional level (i.e. each circuit function - memory, processing, communications, display - forms a separate partition), which in many instances corresponds to the level of an individual VLSI circuit. This enables assembly and disassembly by function (often by individual VLSI) and also replacement, repair, upgrade or expansion by function. Products disassemble also at a functional level, which, it is argued, extends MTBF towards the MTBF for the individual VLSI circuits, and permits reuse of the disassembled circuit blocks in a wide range of alternative applications (i.e. tending to maximise RV).

Low overall volume. The characteristic form factor that results when assemblies are stacked in this way produces robust systems of very low overall volume. A number of applications can benefit directly from these attributes - for example, hand-held data loggers or instrumentation for confined spaces.

Simple snap assembly and disassembly. Carriers and connectors simply snap together during assembly and snap apart for disassembly. Working systems are easily and rapidly assembled, and hand assembly rates of 2-3 systems per minute, using minimal aids and jigs, are possible. Mechanised assembly is expected to result in very high assembly rates. Unlike many other technologies, disassembly is also very simply carried out and yields a set of readily reused connectors and components. Costs and difficulties of disassembly are thus minimised.

Ease of modification. The highly modular nature of the system facilitates alteration or enhancement. For example, the processor unit and service layer could be replaced with a different, or an upgraded processor and interface. Existing memory carriers may be replaced with carriers of higher capacity as appropriate devices become available. This need entail changes only to the

functions. Further, it can only be easily connected to a product presenting a PC interconnection bus (the board has been designed to slot into a particular type of connector implementing a specified bus structure). In practical terms this means that expansion boards removed from PC computers can only be easily reused in other similar PC computer systems. Moreover, the technological advances within the development of the whole of PC systems make the reuse of old technology expansion cards on new mother boards an unattractive proposition.

A central assertion of this paper is that the economics, and hence the attractiveness of reuse of sub-assemblies or components, are crucially influenced by the partitioning scheme adopted and the interconnection system which interconnects the sub-assemblies or components.

Mean Time Between Failures and Residual Value

A further consideration relates to the Mean Time Before Failure (MTBF) and the Residual Value (RV) of the disassembled parts. Individual components have individual MTBFs; however, the MTBF of a sub-assembly often translates into the MTBF of the shortest life component when the costs involved in skilled test and repair mean that it is uneconomic to diagnose faults. The RV of a component or sub-assembly is related to the MTBF, and to the nature and range of alternative uses for the part. The longer the MTBF and the greater the value and range of alternative uses, the greater the RV.

Current Personal Computers disassemble into the following components:-

(1) a small number of high RV components (where the MTBF is the MTBF of the component) and the range and nature of the use of the recovered component is as wide as the original part.

(2) a small number of low RV sub-assemblies (where the MTBF of the sub-assembly is effectively the shortest MTBF of the shortest lived component in the sub-assembly). The fixed bus structure limits alternative use (often to deployment within other PC systems) and rapidly evolving technology within the PC product range limits attractiveness.

(3) a collection of low RV interconnection and support hardware. Alternative applications are again largely restricted to reuse within PC systems.

An Alternative Approach

An alternative approach to partitioning and interconnection can now be examined. In the implementation to be described, electronic systems are partitioned into smaller circuit assemblies of uniform size. Each circuit assembly consists of a conveniently sized substrate or *carrier*, containing a single highly integrated VLSI component, or, if appropriate, a number of less tightly integrated circuits or discrete components. The carriers are then stacked vertically and assembled using a novel form of demountable connector (see Figure 1), in an arrangement described by Anstey (1). The connector provides positive registration for each sub-assembly and once secured, gives the resultant stack considerable strength and rigidity. It offers the designer considerable scope for establishing interconnections between the layers of which the system is comprised. Manufacture of an electronic system is simply a matter of arranging the required carriers into a vertical stack and clamping or fixing the resulting assembly. The upper surface of one carrier is directly connected to the lower surface of an adjacent carrier by means of the connector. This is achieved by a set of independent sprung contacts pressed into retaining channels moulded into the insulating portion of the connector. When a number of carriers are stacked, the contacts align vertically, forming vertical columns of interconnections. In addition, the connector contacts present all signals passing between carriers to the outside of the stack. These characteristics jointly offer a number of unusual possibilities for signal routing. Each column of interconnections in the stacked assembly intersects with every carrier at both its upper and its lower surface. At each intersection, the pattern of signals may be reorganised by attention to the arrangement of circuit tracking on the layer, or by other means.

Evaluation

To explore the effectiveness of this new philosophy for system partitioning, a number of test systems have been designed and evaluated. An embedded computer system based on the PC architecture has formed the principal model for this test programme. The heart of the unit is the F8680 device manufactured by Chips and Technologies, Inc. This device is essentially compatible with the Intel 8088 microprocessor on which the original IBM PC was based, but incorporates a number of powerful features which render it attractive for embedded applications. This single device is capable of implementing the IBM XT interface bus with no additional external circuits; it provides a serial I/O port, a CGA-compatible graphics display controller and a versatile keyboard interface, with support for the emerging PC Card standard. In addition, the F8680 features pipelined operation, has non-multiplexed buses and is able to generate control signals to address up to 64 M Bytes of memory, which may include banks of ROM and static or dynamic RAM.

The embedded PC consists of a number of component carriers and connectors which, when stacked together, form a very compact microprocessor system. The carriers, in order of arrangement in the stack are as follows:-