A COST-EFFECTIVE APPROACH TO 3-D INTERCONNECTION

by Mike Anstey, ICDC Ltd.

Traditionally, semiconductor products have been packaged in the dual-in-line (DIL) style of package. The package provides for the mounting of the semiconductor, and for the interconnection between the semiconductor and the major interconnecting network — the printed circuit board. The DIL package was designed to enable interconnection to an essentially two-dimensional major interconnecting network. The demands of very large scale integration (VLSI) are forcing the reconsideration of the DIL package as the acceptable industry standard and for certain products requiring a large number of signal connections, the DIL package is already unacceptable.

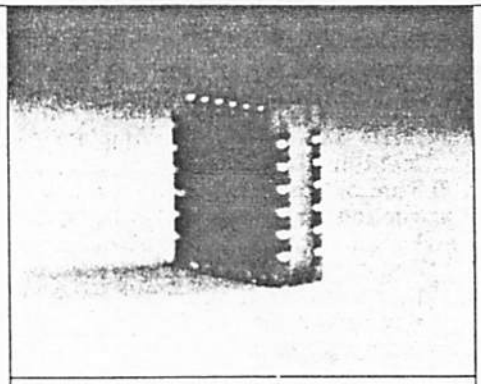
The heir apparent is the chip carrier style of package. Here, the use of all four sides of the package and the reduction in contact pitch, mean that the size of the package can be reduced and the larger number of contact points accommodated.

Chip carriers are at present being interconnected in a similar manner to the DIL package in that the carriers provide interconnection to an essentially two-dimensional major interconnecting network — again the printed circuit board. If a greater complexity of interconnection than that which is obtainable from a single-layer printed circuit is required, then the current solution is to provide a multilayer printed circuit board with vias running between the layers.

The costings of printed circuit boads increase rapidly when the two-dimensional interconnection of a single printed circuit board is extended into three dimensions by the vertical interconnections between the layers of a multilayer board.

This article considers a simpler and much cheaper method of three-dimensional interconnection, which stems from the re-examination of the basic integrated-circuit package, and the requirements of automated assembly related to an appropriately modified integrated-circuit package.

The currently available chip carriers allow two-dimensional interconnection between the semiconductor die and the major interconnecting network. However, if a carrier is constructed which has connecting pads on both upper and lower surfaces (see photograph), then the number of available contacts per carrier is doubled and the carrier itself can become a functional part of a three-dimensional interconnection system. The semiconductor die can be connected to pads on upper or lower surfaces, and signals can enter on one surface of a carrier at a particular point and then emerge or continue from the other surface at another appropriate point. Some signals can enter or leave from one surface while the other surface may be committed to a separate set of signals.



The ability to re-route power, or signal, within a carrier structure (Fig. 1) can be considered as the 'modularising' of the complexity of a printed circuit board (i.e. the re-routing of power, or signal, now implemented by means of a printed circuit board, is effectively incorporated into the basic semiconductor package).

It now becomes feasible to consider much simpler, more regular methods of interconnection between component packages than the customised circuit board. The degree of re-routing necessary depends on the pin-outs of the semiconductor die to be employed in the system. In some structures (e.g. memory arrays or systems employing die designed specifically) there may be little or no re-routing required.

At present, the mounting of such carriers into a standardised interconnecting rack or interconnection by means of standardised interconnecting spacers is considered to be the best of the alternatives — no longer do the interconnecting structures have to be customised, and, therefore, they can be mass produced in volume with resulting economies of scale.

Commercial electronics assembly methods are largely cost driven.

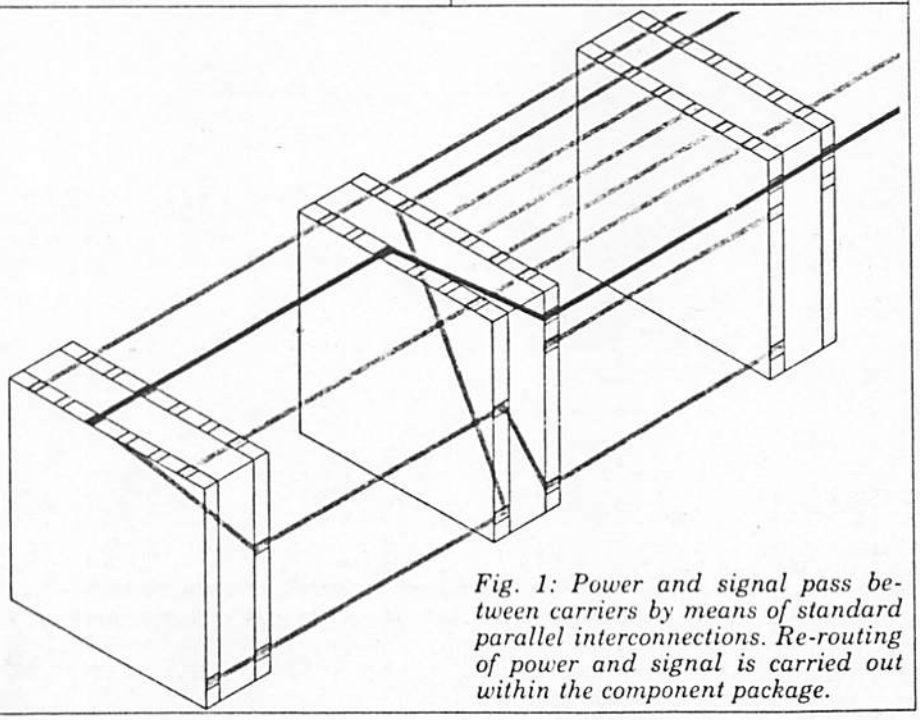


Fig. 1: Power and signal pass between carriers by means of standard parallel interconnections. Re-routing of power and signal is carried out within the component package.