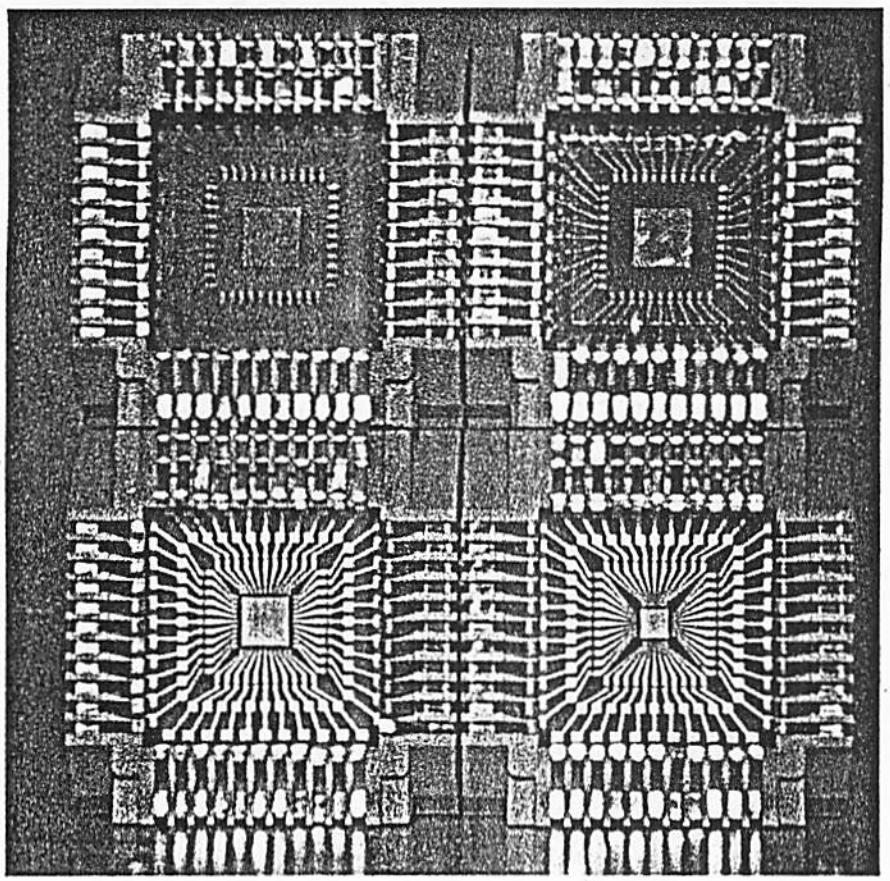
A 3-D System for Interconnection Meets the Challenge of High Density Packaging

Changes in the nature of individual components have forced changes not only in component package design but ultimately the traditional method of system construction.



1. The use of a standardized *three-dimensional matrix structure for interconnection, such as the Chip Rack prototype shown, coupled with rapid hard-tooled automated assembly holds the potential of substantial cost reductions. (I.C.D.C./Dowty Group)*

By Mike Anstey, I.C.D.C., Ltd.,
Wokingham, Berkshire, England

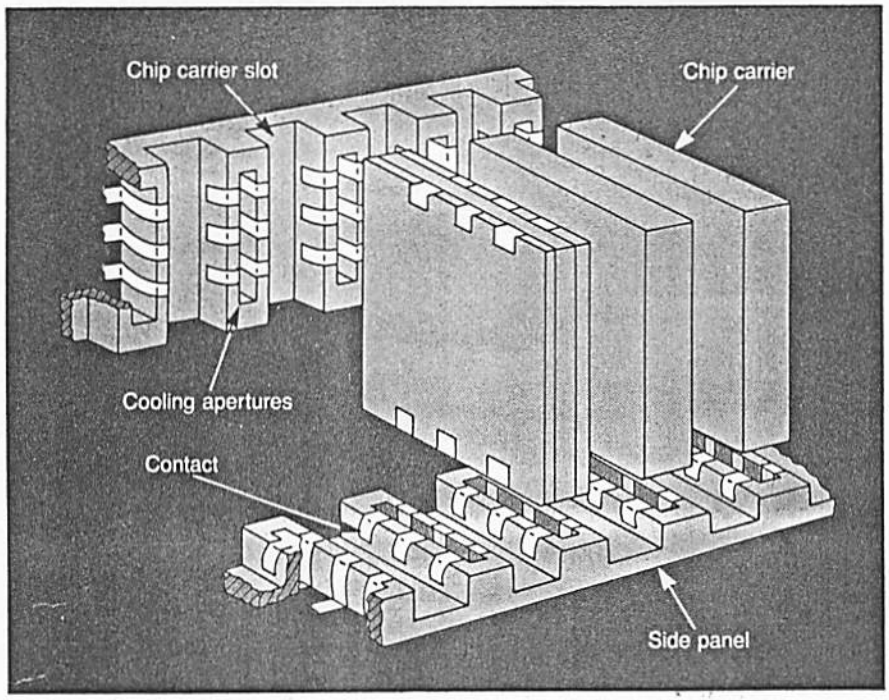
The use of standardized interconnecting structures, coupled with rapid hard-tooled automated assembly, holds the potential of substantial cost reductions. Such a system should not only facilitate automated assembly, but also anticipate the outcome of established trends within the semiconductor industry.

Trends

A project at A.C.I.C., which sprang out of a proposal for such a system, and ultimately yielded a prototype of the product tradenamed Chip Rack, (rights assigned to Dowty-UECL in the U.K.) considered six major trends:

Increasing scale of integration. Recent advances in VLSI technology have enabled the resolution of complex subassemblies into individual components, and as a result, it seems reasonable to assume that many products will ultimately be reduced to a small number of VLSI packages requiring interconnection to each other and to the external world.

Increasing availability and falling costs of custom and semicustom circuits. As more companies offer custom and semicustom product lines and CAD facilities improve, it was expected that prices would fall. Also, ease of design, coupled with increased availability, would result in widespread usage. Customer-specific cir-



***4. The use of both racking** (shown) and interconnecting spacers are two of the more promising systems to be evaluated in the Chip Rack project.*

place all the components.

• The placing of flat component packages onto the flat surface of a PCB may effectively insulate one of the major heat-dissipating surfaces unless the board is of more expensive multilayer construction.

• Solder fractures can occur when leadless packages are soldered onto PCBs if the material of the carrier and the PCB expand and contract at different rates during thermal cycling.

• Increased packing densities often necessitate the use of expensive multilayer boards in order to implement the complexity of interconnection within the reduced board area.

Specifics evaluated

A number of different forms of interconnection systems are worth evaluating in such a project. The use of interconnecting racking or interconnecting spacers could certainly be said to be two of the most promising. (see Figs. 4a and 4b). All systems evaluated should exhibit the following features:

1. Interconnections between carriers are accomplished by means of standardized regular interconnection structures, no longer requiring customization for each design. They can therefore be mass-produced at low cost. However, the structures, coupled with the carrier, enable the complex interconnecting patterns obtainable from a PCB card to be implemented.

2. The form of the interconnecting structure is constant for each application. The assembling machine no longer needs to be software-controlled but can be hard-tooled and carriers may be simultaneously placed into the structure. The capital cost of automated assembly can therefore be substantially reduced and assembly times reduced to a few seconds.

3. The interconnecting structure supports carriers in the vertical plane and skeletonization of the racking permits effective cooling from both sides of the semiconductor package. The design of the interconnecting conductors is such that the surface of the interconnecting structure behaves as a heat sink.

4. The perforated interconnecting structure permits testing at any point down the structure and also permits power or signals to pass between structures at appropriate nodes. Structures can therefore be linked in series or in parallel, according to the complexity of interconnection required. Structures linked in parallel can be built into a honeycomb form to support complex interconnections.

5. The interconnecting structure implements interconnections of minimal length and of considerable symmetry in order to reduce propagation delays and enable increased performance.

6. The structure is capable of ensuring positive location of components as they are inserted. Solder preforms enable controlled reflow under vapor phase.

7. Power or selected signals may be bussed down the structure; alternatively, the intersection of each carrier may break the path of power or signal to permit rerouting at the point of intersection. Limited rerouting may take place within a component-carrying carrier; alternatively, carriers containing rerouting networks may be inserted. These are most cost-effectively implemented by incorporation into the custom or semicustom designs within the system. In some applications, (e.g., byte-wide memory arrays) there may be little or no rerouting necessary. ■

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