Transputers find a new home

by Simon Parry

Dowty Electronic Interconnect is building a transputer array based upon its innovative Chiprack chip carrier system.

The array uses 16 T414 transputers arranged in four equal vertical stacks. Each transputer has 256kbit of dedicated dynamic ram and all transputer links in each stack are configurable.

The basic building block of the Chiprack is a leadless chip carrier with signal contacts on upper and lower faces. These carriers are interconnected using racking spacers that maintain contiguous signals. So signals may pass through the spacer or may be available on only one side of the spacer.

Dowty built a prototype Z80 system that illustrated the principle. A stack comprised clock and reset logic at the base board level and, moving up the stack, parallel I/O, the Z80 microprocessor, memory address decode logic, eeprom and then ram.

The power and data signals lines extend from the board through all levels of the stack but others connect only specific levels: the address lines only connect the microprocessor and memory levels, the clock and reset lines move downwards from the microprocessor.

In the transputer array each transputer is sited in a 104 way chip carrier.

The dedicated memory sits above its transputer and all the address and control lines from each transputer are terminated there.

The clock and reset lines continue through the stack and all the link lines for all the transputers arrive at a hardwired, 32pin socket that sits on the stack top. The links from the bottom most transputer together with one link from each of the other transputers are connected to the motherboard in addition to a few other signals such as even acknowledge and request.

The 32pin socket can be used to change the architecture of the links.

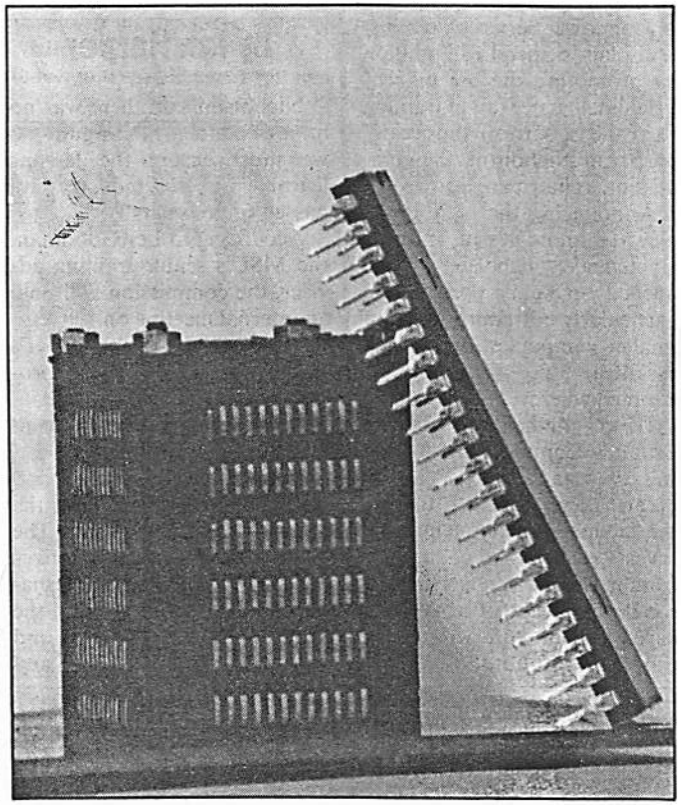
Nick Becket, a senior project engineer at Dowty, said he had hoped to have a working prototype of the transputer array at Internepcon at Brighton this week.

"But production of the motherboard and chip carriers has been a bit protracted," he said.

Becket is confident there will be a working example of the array within six weeks.

Becket said the prototype would run a standard graphics display software package from Inmos but that "we hope that with 16 transputers it will run considerably faster".

"This is the first stage.... Our goal is to reduce the size of the Chiprack to within 10 or 15% of the footprint of an ordinary chip package."



A complete Z80 system in comparison with a single 40pin, dual in line package.

SGS updates asic thinking

One of today's trends in asic design is to improve the usefulness of macrocells an engineer will not increase beyond that," Miller said. The memory is using a poly short out tech-